Power Quality Improvement using VSI based Unified Power Quality Conditioner (UPQCC)

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Abstract—Power quality has become a crucial factor today due to wide application of power electronics based equipment. Conventional equipment for enhancement of power quality is becoming inadequate. Unified power quality conditioner (UPQC) is one modern device which deals with voltage and current imperfections simultaneously. In this paper, an attempt has been made to model the UPQC for voltage and current compensation with the help of two different control schemes. The current and voltage harmonics as well as voltage sag and swells compensation are shown.

Keywords—Power Quality, Active power Filter, Modeling of UPQC, simulation.

I. INTRODUCTION
Wide application of power electronic based equipment has resulted in a serious impact on the nature of electric power supply. Smooth uninterrupted sinusoidal voltage at desired magnitude and frequency should always be provided to the consumers. On the other hand consumers should draw sinusoidal current [1]. Efforts are being made by many researchers for the effective improvement of power quality. UPQC is considered as the most powerful solution to the problems arising due to power quality. It is adequate enough to take care of supply voltage disturbances like voltage sag/swells, voltage flickers, load reactive power as well as voltage and current harmonics. The UPQC can also be named as the universal active power line conditioner, universal power quality conditioning system and also universal active filter. It is a cascade connection of series and shunt active power filter (APF) connected through a common DC link capacitor [2].

The series APF is coupled to the supply line through a series transformer. The series APF prevents the source side voltage disturbances from entering into the load side to make the load voltage at desired magnitude and frequency [2]. Whereas the shunt APF connected in parallel across the load confines the current related problems to the load side to make the current from the source purely sinusoidal [3].

In this manuscript two different control schemes are used for series and shunt APF. The control algorithm is simulated in MATLAB/SIMULINK.

II. UPQC CONTROL STRATEGY
The detailed structure of UPQC is described in Fig. 1. The UPQC comprises two voltage source inverters connected through a common dc link capacitor. The series inverter coupled to the line in series compensates for the voltage related problems such as voltage sag/swells, voltage flickers and voltage harmonics. The shunt inverter is treated as current source and is connected in shunt with the same AC line to mitigate problems related to current such as current harmonics, load reactive power and control of the dc link capacitor voltage. The DC link capacitor expedites the sharing of active power among the two inverters.

FILTER DESIGN

a) Low pass filter
Low-pass filters are commonly used to implement antialias filters in data-acquisition systems. Design of second-order filters is the main topic of consideration. Filter tables are developed to simplify circuit design based on the idea of cascading lower order stages to realize higher-order filters. The tables contain scaling factors for the corner frequency and the required Q of each of the stages for the particular filter being designed. This enables the designer to go straight to the calculations of the circuit-component values required.

Filter Characteristics
If an ideal low-pass filter existed, it would completely eliminate signals above the cutoff frequency, and perfectly pass signals below the cutoff frequency. In real filters, various trade-offs
are made to get optimum performance for a given application.

**Butterworth** filters are termed maximally-flat-magnitude-response filters, optimized for gain flatness in the pass-band. The attenuation is \(-3\) dB at the cutoff frequency. Above the cutoff frequency the attenuation is \(-20\) dB/decade/order. The transient response of a Butterworth filter to a pulse input shows moderate overshoot and ringing.

**Bessel** filters are optimized for maximally-flat time delay (or constant-group delay). This means that they have linear phase response and excellent transient response to a pulse input. This comes at the expense of flatness in the pass-band and rate of rolloff. The cutoff frequency is defined as the \(-3\)-dB point.

**Chebyshev** filters are designed to have ripple in the pass-band, but steeper rolloff after the cutoff frequency. Cutoff frequency is defined as the frequency at which the response falls below the ripple band. For a given filter order, a steeper cutoff can be achieved by allowing more pass-band ripple. The transient response of a Chebyshev filter to a pulse input shows more overshoot and ringing than a Butterworth filter.

**Active Filtering** An active filter reduces distortion in the line current by supplying the harmonics components in load current. The maximum value of the filter current is obtained at 60˚. The Voltage rating of the switches is equal to the D.C bus bar voltage within the converter of the active filter. The voltage developed by the active filter is different from the source voltage drop across inductance. If this inductance is small due to the choice of a high switching frequency, then the voltage is approximately equal to the source voltage. [10].

**Hybrid Filtering** The passive filter absorbs all the harmonics in the load current, while the series active filter decouples the utility from the load and passive filters at the harmonics frequencies. Thus the load and the passive filter draw only fundamental frequency currents from the utility. Since the load is a six-pulse rectifier, the shunt passive filter network in each phase is assumed to consist of series-tuned filter, tuned to the 5th and 7th harmonics, with a high pass filtering concept. The total reactive power supplied by the passive filter network at the fundamental frequency is taken to be 20% of the load power. This allows a displacement power factor under light load conditions. The resistors in the series-tuned filter branches are calculated by assuming the quality factor at their respective harmonic frequencies, to be 100. The selection of component is based on the considerations of out lined nth harmonic component in the load current is calculated. [10]

**OPERATING PRINCIPLE OF UPQC**

The basic components of the UPQC are two voltage source inverters (VSIs) sharing a common dc storage capacitor, and connected to the power system through coupling transformers. One VSI is connected to in shunt to the transmission system via a shunt transformer, while the other one is connected in series through a series transformer.

![Fig. 1 operation of UPQC](image)

The series inverter is controlled to inject a symmetrical three phase voltage system (Vse), of controllable magnitude and phase angle in series with the line to control active and reactive power flows on the transmission line. So, this inverter will exchange active and reactive power with the line. The reactive power is electronically provided by the series inverter, and the active power is transmitted to the dc terminals. The shunt inverter is operated in such a way as to demand this dc terminal power (positive or negative) from the line keeping the voltage across the storage capacitor Vdc constant. So, the net real power absorbed from the line by the UPQC is equal only to the losses of the inverters and their transformers. The remaining capacity of the shunt inverter can be used to exchange reactive power with the line so to provide a voltage regulation at the connection point.

The two VSIs can work independently of each other by separating the dc side. So in that case, the shunt inverter is operating as a STATCOM that generates or absorbs reactive power to regulate the voltage magnitude at the connection point. Instead, the series inverter is operating as SSSC that generates or absorbs reactive power to regulate the current flow, and hence the power low on the transmission line.

The UPQC has many possible operating modes. In particular, the shunt inverter is operating in such a way to inject a controllable current, ish into the transmission line. The shunt inverter can be controlled in two different modes:

**VAR Control Mode:** The reference input is an inductive or capacitive VAR request. The shunt inverter control translates the var reference into a...
corresponding shunt current request and adjusts gating of the inverter to establish the desired current. For this mode of control a feedback signal representing the dc bus voltage, Vdc, is also required.

Automatic Voltage Control Mode: The shunt inverter reactive current is automatically regulated to maintain the transmission line voltage at the point of connection to a reference value. For this mode of control, voltage feedback signals are obtained from the sending end bus feeding the shunt coupling transformer.

The series inverter controls the magnitude and angle of the voltage injected in series with the line to influence the power flow on the line. The actual value of the injected voltage can be obtained in several ways.

Direct Voltage Injection Mode: The reference inputs are directly the magnitude and phase angle of the series voltage.

Phase Angle Shifter Emulation mode: The reference input is phase displacement between the sending end voltage and the receiving end voltage. Line Impedance Emulation mode: The reference input is an impedance value to insert in series with the line impedance.

Automatic Power Flow Control Mode: The reference inputs are values of P and Q to maintain on the transmission line despite system changes.

Voltage source inverter

The voltage source inverter topology uses a diode rectifier that converts utility/line AC voltage (60 Hz) to DC. The converter is not controlled through electronic firing like the CSI drive. The DC link is parallel capacitors, which regulate the DC bus voltage ripple and store energy for the system. The inverter is composed of insulated gate bipolar transistor (IGBT) semiconductor switches. There are other alternatives to the IGBT: insulated gate commutated thyristors (IGCTs) and injection enhanced gate transistors (IEGTs). This paper will focus on the IGBT as it is used extensively in the MV VSI drives market. The IGBT switches create a PWM voltage output that regulates the voltage and frequency to the motor.

Current source inverter

The way each of the drive building blocks operates defines the type of drive topology. The first topology that will be investigated is the current source inverter (CSI). The converter section uses silicon-controlled rectifiers (SCRs), gate commutated thyristors (GCTs), or symmetrical gate commutated thyristors (SGCTs). This converter is known as an active rectifier or active front end (AFE). The DC link uses inductors to regulate current ripple and to store energy for the motor. The inverter section comprises gate turn-off thyristor (GTO) or symmetrical gate commutated thyristor (SGCT) semiconductor switches. These switches are turned on and off to create a pulse width modulated (PWM) output regulating the output frequency.

III. SIMULATION RESULTS

The proposed control scheme is developed in MATLAB/SIMULINK environment. Simulation parameters as specified in [2] have been used for this purpose. In order to introduce nonlinear load a three phase diode bridge with RL load on dc side is used. The simulation results for compensation of voltage sag/swell, compensation of current and voltage harmonics are presented voltage. This distortion is done deliberately to study the harmonic compensating capability of UPQC to source voltage. The series APF injects an out-of-phase voltage with 5th and 7th harmonic which is the difference between the desired load voltage and actual supply voltage after 0.1sec as realized in Fig. 6(b). The load voltage profile can be seen from Fig. 6 (c) which is free from any distortion. Current harmonics generated by the nonlinear load is compensated by the Shunt APF. The load current can be seen in Fig.6 (d). The shunt APF injects a current in such a manner that the source current (Fig. 6(e)) becomes sinusoidal. The improved source current profile is observed in Fig. 6(f). The shunt APF also maintains the dc link voltage at reference value as seen in Fig. 6(g).
B. Voltage sag and current harmonic compensation

The simulation result of voltage sag and current harmonic compensation is observed in Fig. 9. A sag (20%) is introduced to the supply voltage at 0.1 sec and lasts till 0.25 sec. as shown in Fig. 9(a). Fig. 9(b) shows the injected in phase voltage from the series APF. This voltage is the difference between the desired voltage at the load side and the actual voltage at the source side. Thus, UPQC is able to maintain the desired level of the load voltage (Fig. 9(c)) so that the source side sag in voltage does not affect the load side voltage. The UPQC requires some supply of active power so that the in-phase voltage can be injected. This power is drawn from the source by shunt inverter, by taking extra current component to keep the DC link voltage (Fig. 9(g)) at fixed level. If it is not maintained, the DC link voltage will drop to very low value in very few cycles. The current drawn by shunt inverter is shown in Fig. 9(e) (between time 0.1 sec. and 0.25 sec.), and the consequent increase in the magnitude of the source side current is also noticed accordingly in Fig. 9(f).
C. Voltage swell and current harmonic compensation

The simulation result of voltage swell compensation is shown in Fig. 10. A swell (20%) is introduced to the supply voltage at 0.1 sec. and lasts till 0.25 sec as shown in Fig. 10(a). The voltage sag and swell conditions are opposite to each other. Therefore, during a source side voltage swell, the series APF now injects out-of phase voltage equal to the difference between the desired voltage at the load side and the actual voltage at the source side (Fig. 10(b)). Hence, the UPQC cancels the increased source voltage that may appear at the load side and keeps the desired level of the load voltage (Fig. 10(c)). The increase in source side voltage reflects that the utility is supplying some extra power to the load. This may damage equipments and loads due to the increase in current drawn by them. At the same time, the rise in source voltage results in the increase of the DC link voltage. Under aforesaid situation, out-of phase fundamental current component is injected by the shunt APF (Fig. 10(e)) between instants 0.1 sec and 0.25 sec. to keep fixed DC link voltage level. Accordingly there is a consequent decrease in the magnitude of the source side current (Fig. 10(f)).

IV. CONCLUSION

This work proposes a control scheme for UPQC based on hysteresis voltage and current controller. In this scheme the series APF and the shunt APF of the UPQC are controlled by the combination of UVT and instantaneous p-q theory. The UPQC model was developed and simulated in MATLAB/SIMULINK environment. It can be observed from the results obtained through simulation that the supply side voltage sag/swell, harmonic as well as the load side current harmonics are easily taken care of by the use of the proposed control scheme. It can also be noticed from the results that the supply side current and load voltage harmonics levels are well below the IEEE 519 standards [10].

REFERENCES


