Low-Power and Area-Efficient Shift Register Using Pulsed Latch

Mutum Arnica & Mr. Amit
SRM university

Abstract: With so many events happening in the world at a very fast pace the human race is in search for new technological advancements. There is a high demand for minutely packed power devices that have higher efficiency of area which has lead the industry of VLSI to venture into the unknown. As technology moves into these levels the power management requirement of the devices rise. This paper proposes allow power and area-efficient shift register using pulsed latches. The area and power consumption are made to reduce by substituting flip-flops with pulsed latches. The timing difficulty in the pulsed latches that originate out of the use of conventional single pulsed clock signal is taken care of by the use of multiple non-overlap delayed pulsed clock signals. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

INTRODUCTION:
Technology has invaded into the life of human beings to such deep extent that today everyone has a wish for smaller faster fancier gadgets. This wish has been granted to them by the technological developments in the field of VLSI technology.

A SHIFT register is the basic building block in a VLSI circuit. Shift registers find them to be use full commonly in many applications, such as digital filters, communication receivers, and image processing ICs. Now a days, as there is high demand of images with utmost clarity the size of the image data continues to increase, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register. A 16-megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations.

BASIC CONCEPT:
The designing of a shift register is quite simple. An n bit shift register is composed of series connected N data flip-flops.The speed of the flip flops is of no major constraint here as there are no connections between the shift registers and flip flops. The smallest flip flop is enough to drive the requirement of the shift register and for this same reason the pulsed latches have replaced the flip flops as they are much smaller in size Vis a Vis the flip flops there by reducing power consumption. Although there are some drawbacks like that of the timing problem, which is easy to overcome by the use of multiple clocked pulses instead of a single simple pulsed clock. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

REVIEW FLIP-FLOPS AND LATCHES:
In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information. A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

Flip-flops and latches are used as data storage elements. A flip-flop stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero". Such data storage can be used for storage of state, and such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal.
ARCHITECTURE:

The paper architecture consists of three things-
1. Proposed shift register
2. Design implementation
3. Circuit Design and waveform using virtuso

Proposed shift register –

A master-slave flip-flop using two latches in Fig. 3 can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal fig 4. For the pulsed clock signal all the pulsed latches share the pulse generation circuit. Due to this sharing of the pulse generation circuit the area and power consumption of the circuits reduces to almost half of the master slave flip flop.

It has a drawback that the pulsed clock generator can’t be used directly on this circuit due to its timing problems. To overcome this various steps can be implemented such as –

- to add delay circuits between latches
- use multiple non-overlap delayed pulsed clock signals

All though both the above mentioned methods solve the timing problem the delay circuits present challenge in the area and power consumption domain, so it is best in the interest of low power and area designing to make use of the non overlapping multiple delayed pulse clock signals.
Design implementation –

While designing any circuit or chip it’s important to consider various factors responsible for it to be implemented in real life. The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flops. Therefore, the area and power consumption are more important than the speed for selecting the flip-flop. The proposed 4-bit shift register uses four latches and it performs shift operation with five non overlap delayed pulse clock signals (CLK_pulse<1:4 and CLK_pulse<T>). In the 4 bit shift register, four latches store four bit data (Q1-Q4). The sequence of the pulsed clock signals is in the opposite signal of the four latches.

The pulse clock signal CLK_pulse(1:4) updates the four latch data Q4 to Q1 sequentially. The latches Q2-Q4 receive data from Q1-Q3 but the first latch Q1 receives data from the input of the first register (IN).

Circuit Design

SISO SHIFT REGISTER

Waveform of SISO
SIPO SHIFT REGISTER

PIPO SHIFT REGISTER

Waveform of SIPO

Waveform of PIPO
CONCLUSION:
In this paper the main motive is to design a low power and area efficient shift register which uses pulsed latches instead of conventional flip flops and there by saves 37% area and 44% power compared to the conventional shift register with flip-flops.

REFERENCES:


