A PWM Approach for 3-Level and 5-Level H-Bridge Cascaded Inverters under Unbalanced Dc-Link Sources

M. Anilkumar Naik¹ & K. Leleedhar Rao²
¹PG Student, EEE, Sree Vidyanikethan Eng. College, Andhra Pradesh, India.
²Assistant Professor, EEE, Sree Vidyanikethan Eng. College, Andhra Pradesh, India.

Abstract: For a medium voltage grid, it's troublesome to connect power semiconductor switches directly. As a result, a multilevel power device structure has been introduced as an alternate in high power and medium voltage things. As a price effective solution, multilevel device that not only achieves high power ratings, however, conjointly enables the utilization of low power application in renewable energy sources, may be simply interfaced to a structure device system. During this paper a carrier-based PWM strategy to balance line to line output voltages and to maximize the linear modulation range wherever the output voltage are often linearly controlled in the multilevel cascaded inverters in operation below unbalanced dc-link conditions is projected. In unbalanced dc-link conditions, the maximum synthesizable voltage in each phase is not uniform. Consequently, the linear modulation range is reduced, and a major output voltage imbalance might occur as output voltage references increase. So as to analyze the imbalance impact, the voltage vector space for the MLCI is evaluated thoroughly. After that, a neutral voltage modulation (NVM) strategy is projected to attain output voltage balancing as well as to extend the linear modulation range up to the most accessible point. Within the projected technique, the neutral voltage reference, that considers a zero sequence voltage to compensate the output voltage imbalance, and an offset voltage to increase the linear modulation range are easily obtained through easy arithmetic calculations.

Keywords: MLCI (multilevel cascaded inverters), PWM (pulse width modulation), SVPWM (space vector pwm), NVM (neutral voltage modulation).

1. Introduction

Multilevel inverters change the synthesis of a sinusoidal output voltage from many steps of voltages. For this reason, multilevel inverters have low dv/dt characteristics and usually have low harmonics within the output voltage and current. Additionally, the switching of very high voltages are often achieved by stacking multilevel inverter modules [2]. Because of these benefits, multilevel inverters are applied in numerous application fields [12]-[14]. Among numerous topologies for multilevel inverters, the multilevel cascaded inverter (MLCI) structure is one among the distinguished topologies due to its easy structure for modularization and fault-tolerant capability. Therefore, MLCIs are used for several applications, like dynamic voltage restorer, static synchronous compensator (STATCOM), high-voltage energy storage device, photovoltaic inverters, medium-voltage drives, electrical vehicle (EV) traction drives, and then on [17]-[20]. In MLCI applications, a modulation strategy to get gating signals is extremely crucial to attain high-performance control. Concerning this issue, several studies are conducted, and that they are roughly categorized into multilevel selective harmonic elimination pulse width modulation (SHEPWM), multilevel carrier-based PWM, and multilevel space vector PWM (SVPWM) strategies. Generally, a carrier-based PWM or SVPWM is most popular in applications like motor drives, wherever dynamic properties are important, whereas SHEPWM is preferred in some dynamic static power conversion applications [15]. An SVPWM technique has been studied to cover the over modulation range in the multilevel inverter.

To reduce the common-mode voltage, a multilevel SVPWM has been projected. The series SVPWM technique has been reported to simply implement SVPWM for the MLCI. An SVPWM is projected for hybrid inverters consisting of neutral point clamp and H-bridge inverters to enhance output voltage quality and efficiency [3]-[5]. As with two-level inverters, it's conjointly attainable to implement carrier-based SVPWMs which are similar to traditional SVPWMs by injecting a common offset voltage to the three-phase references. Some strategies to calculate the offset voltages to attain the optimum space vector switching sequence are addressed. The performances of a carrier-based
PWM and an SVPWM are compared, and a PWM scheme is projected to get an best output voltage within the multilevel inverter. On the other hand, MLCIs need separated dc links. Therefore, if there are one or a lot of faults present in the dc links in each phase, or if the voltage magnitudes of the dc links are unequal, the output voltage of the MLCI is often unbalanced without proper compensation. To resolve this issue, some studies are conducted [7]-[10].

However, the series association of switch power devices have huge issues, like, un-equal distribution of applied device voltage across series-connected devices that will make the applied voltage of individual device much higher than their obstruction voltage throughout transient and steady-state switching operation. As alternatives to effectively solve the preceding issues, many circuit topologies of multilevel inverter are researched and utilized. The output voltage of the multilevel inverter has several levels synthesized from many DC voltage sources. the quality of the output voltage gets improved because the range of voltage levels will increase, therefore the amount of output filters are often decreased .

A multilevel converter are often implemented in many various ways in which the only techniques involve the parallel or series connection of standard converters to make the multilevel waveforms. More advanced structures effectively insert converters within converters. The voltage or current rating of the multilevel converter becomes a multiple of the individual switches, and so the power rating of the converter will exceed the limit imposed by the individual switching devices.

In this paper, a carrier-based PWM strategy to balance line to line output voltages and to maximize the linear modulation range, wherever the output voltage can be linearly controlled within the MLCI operating under unbalanced dc-link conditions is projected. In unbalanced dc-link conditions, the most synthesizable voltage in each phase isn't uniform [1]. Consequently, the linear modulation range is reduced, and a major output voltage imbalance might occur as output voltage references increase. in order to analyze the imbalance impact, the voltage vector space for the MLCI is evaluated thoroughly. From this analysis, the theory behind the output voltage imbalance is explained, and therefore the maximum linear modulation range considering unbalanced dc sources is evaluated. After that, a neutral voltage modulation (NVM) strategy is projected to attain output voltage balancing as well as to extend the linear modulation range up to the most reachable point.

2. Simple H-bridge modules

Simple H-bridge module is shown in Fig. 1 in which the dc-link voltage of a single H-bridge module is $V_{dc}$, the output voltage $V_{pm}$ has three states i.e., $V_{dc}$, 0, -$V_{dc}$. By assuming the concept of a switching function, it can be represented as

$$V_{pm} = S_p V_{dc}$$  \hspace{1cm} (1)

Where $S_p$ is a switching function and $p$ can be replaced with $a$, $b$, or $c$, which represent the phases.

For voltage vector space analysis, the main concept is derived from this modest topology, and then, it is prolonged to more levels. In Fig. 1, there are two neutral points $s$ and $n$ in the MLCI. Here, the voltage between the output point of each phase and the neutral point $n$ is defined as the pole voltage. The pole voltages are represented as $v_{an}$, $v_{bn}$, and $v_{cn}$. The voltage between the output point of each phase and the load side neutral point $s$ is specified as the phase voltage. The phase voltages include $v_a$, $v_{bs}$, and $v_{cs}$.

By using this concept, the voltage between the two neutral points is defined as $v_{sn}$ and can be written as

$$v_{sn} = v_{an} + v_{bn} + v_{cn} \hspace{1cm} (2)$$

By using the condition that the sum of all phase voltages is zero as the load does not have a neutral line, $v_{an}$ is rewritten as

$$v_{an} = \frac{1}{3}(v_{bn} + v_{cn}) \hspace{1cm} (3)$$

By substituting eqn (3) into eqn (2), the phase voltage of each phase is represented as follows by using the relationship defined in eqn (1):

$$v_a = \frac{2}{3} S_a V_{dc, a} + \frac{1}{3} S_b V_{dc, b} + \frac{1}{3} S_c V_{dc, c}$$

$$v_b = -\frac{1}{3} S_a V_{dc, a} + \frac{2}{3} S_b V_{dc, b} + \frac{1}{3} S_c V_{dc, c}$$

$$v_c = -\frac{1}{3} S_a V_{dc, a} + \frac{1}{3} S_b V_{dc, b} + \frac{2}{3} S_c V_{dc, c} \hspace{1cm} (4)$$
3. Proposed modulation technique

The extreme synthesizable voltage within the linear modulation range was evaluated under the unbalanced dc link sources. In this section, a method is presented to realize the modulation index within the linear modulation range under these conditions.

3.1 Outmoded offset voltage injection method

The offset voltage injection method is a usual method in 3-phase half-bridge inverter applications. In this an offset voltage is incorporated with phase voltage references to implement various PWM schemes in carrier-based PWM by using the fact that line-to-line voltages are applied to a three-phase load. For example, the offset voltage \( v^*_{sn} \) is injected to the phase voltage references \( v^*_{as} \), \( v^*_{bs} \), and \( v^*_{cs} \) to implement carrier-based SVPWM as in

\[
K_w = \frac{V_{dc, mid} + V_{dc, min}}{2} \quad (7)
\]

Where \( V_{dc, max} \), \( V_{dc, mid} \), and \( V_{dc, min} \) represent the maximum, medium, and minimum voltages among the dc links.

By using eqn (7), the weight factors are calculated as

\[
K_{w-a} = \frac{K_w}{v_{dc-a}}, \quad K_{w-b} = \frac{K_w}{v_{dc-b}}, \quad K_{w-c} = \frac{K_w}{v_{dc-c}} \quad (8)
\]

However, the above-mentioned method cannot increase the linear modulation range in MLCI undergoing unbalanced dc-link conditions.

3.2 Neutral voltage modulation method

If the dc links in an MLCI are unbalanced and the offset voltage injection methods are utilized, the three-phase output voltages might become distorted because the phase voltage reference approaches \( V_{ph, max} \). This can be as a result of the normal strategies which don’t seem to be considering unbalanced dc-link conditions. Therefore, a phase will synthesize an output voltage reference within the linear modulation range, while the other phases may be saturated or entered the over modulation region. During this state, a neutral voltage may be created by the saturated or over modulated section. So as to resolve this issue and to synthesize the output voltage to \( V_{ph, max} \), the NVM technique is proposed. Fig. 2 shows the idea of the proposed NVM technique. Here, a neutral voltage between the two neutral point’s n and s is modulated to compensate the output voltage imbalance caused by unbalanced dc-link conditions. To do this, first, the weight constant \( k_w \) is considered and defined as

\[
K_{w} = \frac{V_{dc, max} + V_{dc, min}}{2} \quad (7)
\]

Then, the pole voltage references \( v^*_{an} \), \( v^*_{bn} \), and \( v^*_{cn} \), which are converted to PWM duty references, are

\[
v_{an}^* = v_{bn}^* = v_{cn}^* \quad (6)
\]

Then, the pole voltage references \( v_{an}^* \), \( v_{bn}^* \), and \( v_{cn}^* \), which are converted to PWM duty references, are

\[
K_w = \frac{V_{dc, mid} + V_{dc, min}}{2} \quad (7)
\]

Where \( V_{dc, max} \), \( V_{dc, mid} \), and \( V_{dc, min} \) represent the maximum, medium, and minimum voltages among the dc links.

By using eqn (7), the weight factors are calculated as

\[
K_{w-a} = \frac{K_w}{v_{dc-a}}, \quad K_{w-b} = \frac{K_w}{v_{dc-b}}, \quad K_{w-c} = \frac{K_w}{v_{dc-c}} \quad (8)
\]

However, the above-mentioned method cannot increase the linear modulation range in MLCI undergoing unbalanced dc-link conditions.

3.2 Neutral voltage modulation method

If the dc links in an MLCI are unbalanced and the offset voltage injection methods are utilized, the three-phase output voltages might become distorted because the phase voltage reference approaches \( V_{ph, max} \). This can be as a result of the normal strategies which don’t seem to be considering unbalanced dc-link conditions. Therefore, a phase will synthesize an output voltage reference within the linear modulation range, while the other phases may be saturated or entered the over modulation region. During this state, a neutral voltage may be created by the saturated or over modulated section. So as to resolve this issue and to synthesize the output voltage to \( V_{ph, max} \), the NVM technique is proposed. Fig. 2 shows the idea of the proposed NVM technique. Here, a neutral voltage between the two neutral point’s n and s is modulated to compensate the output voltage imbalance caused by unbalanced dc-link conditions. To do this, first, the weight constant \( k_w \) is considered and defined as

\[
K_{w} = \frac{V_{dc, max} + V_{dc, min}}{2} \quad (7)
\]

Where \( V_{dc, max} \), \( V_{dc, mid} \), and \( V_{dc, min} \) represent the maximum, medium, and minimum voltages among the dc links.

By using eqn (7), the weight factors are calculated as

\[
K_{w-a} = \frac{K_w}{v_{dc-a}}, \quad K_{w-b} = \frac{K_w}{v_{dc-b}}, \quad K_{w-c} = \frac{K_w}{v_{dc-c}} \quad (8)
\]

However, the above-mentioned method cannot increase the linear modulation range in MLCI undergoing unbalanced dc-link conditions.

3.2 Neutral voltage modulation method

If the dc links in an MLCI are unbalanced and the offset voltage injection methods are utilized, the three-phase output voltages might become distorted because the phase voltage reference approaches \( V_{ph, max} \). This can be as a result of the normal strategies which don't seem to be considering unbalanced dc-link conditions. Therefore, a phase will synthesize an output voltage reference within the linear modulation range, while the other phases may be saturated or entered the over modulation region. During this state, a neutral voltage may be created by the saturated or over modulated section. So as to resolve this issue and to synthesize the output voltage to \( V_{ph, max} \), the NVM technique is proposed. Fig. 2 shows the idea of the proposed NVM technique. Here, a neutral voltage between the two neutral point’s n and s is modulated to compensate the output voltage imbalance caused by unbalanced dc-link conditions. To do this, first, the weight constant \( k_w \) is considered and defined as

\[
K_{w} = \frac{V_{dc, max} + V_{dc, min}}{2} \quad (7)
\]

Where \( V_{dc, max} \), \( V_{dc, mid} \), and \( V_{dc, min} \) represent the maximum, medium, and minimum voltages among the dc links.

By using eqn (7), the weight factors are calculated as

\[
K_{w-a} = \frac{K_w}{v_{dc-a}}, \quad K_{w-b} = \frac{K_w}{v_{dc-b}}, \quad K_{w-c} = \frac{K_w}{v_{dc-c}} \quad (8)
\]

However, the above-mentioned method cannot increase the linear modulation range in MLCI undergoing unbalanced dc-link conditions.

3.2 Neutral voltage modulation method

If the dc links in an MLCI are unbalanced and the offset voltage injection methods are utilized, the three-phase output voltages might become distorted because the phase voltage reference approaches \( V_{ph, max} \). This can be as a result of the normal strategies which don't seem to be considering unbalanced dc-link conditions. Therefore, a phase will synthesize an output voltage reference within the linear modulation range, while the other phases may be saturated or entered the over modulation region. During this state, a neutral voltage may be created by the saturated or over modulated section. So as to resolve this issue and to synthesize the output voltage to \( V_{ph, max} \), the NVM technique is proposed. Fig. 2 shows the idea of the proposed NVM technique. Here, a neutral voltage between the two neutral point’s n and s is modulated to compensate the output voltage imbalance caused by unbalanced dc-link conditions. To do this, first, the weight constant \( k_w \) is considered and defined as

\[
K_{w} = \frac{V_{dc, max} + V_{dc, min}}{2} \quad (7)
\]

Where \( V_{dc, max} \), \( V_{dc, mid} \), and \( V_{dc, min} \) represent the maximum, medium, and minimum voltages among the dc links.

By using eqn (7), the weight factors are calculated as

\[
K_{w-a} = \frac{K_w}{v_{dc-a}}, \quad K_{w-b} = \frac{K_w}{v_{dc-b}}, \quad K_{w-c} = \frac{K_w}{v_{dc-c}} \quad (8)
\]

However, the above-mentioned method cannot increase the linear modulation range in MLCI undergoing unbalanced dc-link conditions.
consider the role of the weightfactors $K_{w_a}$, $K_{w_b}$, and $K_{w_c}$, which are inversely proportional to the corresponding dc-link voltages. For convenience, let us assume that the magnitudes of the dc-link voltage are following the relationship:

$$V_{dc,a} < V_{dc,b} < V_{dc,c}$$  \hspace{1cm} (12)

Then, from eqn (8) and eqn (11)

$$K_{w_a} > K_{w_b} > K_{w_c} \quad K_{w_{a,b}} K_{w_{c'}} < 1 \quad (13)$$

Eqn (13) gives

$$|v'_{a2}| > |v'_{b2}|$$
$$|v'_{b2}| < |v'_{c2}|$$
$$|v'_{c2}| < |v'_{a2}|$$  \hspace{1cm} (14)

From eqn (11) and eqn (14), it can be recognized that, if $v'_{a2}$, whose dc-link voltage is less than the others, is corresponding to $v'_{\text{max}}$ or $v'_{\text{min}}$, the absolute value of $v'_{a2}$ is greater than $v'_{b2}$ in eqn (5). On the other hand, the final pole voltage references $v'_{a2}$, $v'_{b2}$, and $v'_{c2}$ are calculated by subtracting $v'_{sn}$ from the original phase voltage references $v'_{a}$, $v'_{b}$, and $v'_{c}$ as in eqn (10). From the reasoning, in this example, it is supposed that, if $v'_{a2}$ is corresponding to $v'_{\text{max}}$, then the final pole voltage references $v'_{a2}$, $v'_{b2}$, and $v'_{c2}$ are less than the original pole voltage references which are not considering $v'_{sn}$ but $v'_{sn}$. On the contrary, if $v'_{c2}$ is $v'_{\text{max}}$, then the final pole voltage references are greater than the original pole voltage references [8], [9]. By using this principle, the proposed method reduces the portion of the phase whose dc-link voltage is smaller than the others and increases the utilization of the phase in which the dc-link voltage is greater than those of the other phases. However, as it can be seen in eqn (11), $v'_{a2}$ does not affect the line-to-line voltages. Therefore, the line-to-line voltage is the same as the one derived from the original phase voltage reference. From this analysis, the proposed method enables the maximum synthesizable modulation index in the linear modulation range under the unbalanced dc-link conditions to be achieved. In addition to this, if all of the dc-link voltages are well balanced so that $V_{dc,a}$, $V_{dc,b}$, and $V_{dc,c}$ are equal to $V_{dc}$

$$V_{dc_{\text{mid}}} = V_{dc_{\text{min}}} = V_{dc}$$  \hspace{1cm} (15)

By substituting eqn (15) into eqn (9), eqn (13)

$$K_w = \frac{V_{dc_{\text{mid}}}}{V_{dc_{\text{min}}}} = \frac{V_{dc}}{V_{dc_{\text{mid}}}}$$  \hspace{1cm} (16)

Eqn (16) shows that the proposed method gives the same voltage references as the traditional method under balanced dc-link conditions.

4. Duty calculation

In Fig. 2, the final voltage references are entered to the duty reference calculation block. In this block, the duty references of each H-bridge module are calculated as follows:

$$d'_{a1} = d'_{a2} = \cdots = d'_{aN} \text{ with } v_{a2}'$$
$$d'_{b1} = d'_{b2} = \cdots = d'_{bN} \text{ with } v_{b2}'$$
$$d'_{c1} = d'_{c2} = \cdots = d'_{cN} \text{ with } v_{c2}'$$

4. Duty calculation

In Fig. 2, the final voltage references are entered to the duty reference calculation block. In this block, the duty references of each H-bridge module are calculated as follows:

$$d'_{a1} = d'_{a2} = \cdots = d'_{aN} \text{ with } v_{a2}'$$
$$d'_{b1} = d'_{b2} = \cdots = d'_{bN} \text{ with } v_{b2}'$$
$$d'_{c1} = d'_{c2} = \cdots = d'_{cN} \text{ with } v_{c2}'$$

The calculated duty references are compared to PS carriers to generate gating signals, as shown in Fig. 3. It should be noted that the duty references for each H-bridge in each phase are shared in the PS modulation.

5. Simulation of Proposed NVM method

A simple one-by-three configuration of MLCI model is built in Matlab Simulink. The three-phase RL load with $R = 0.1\Omega$ and $L = 1mH$ is employed. The dc-link voltages considered for each phase are $V_{dc,a} = 15V$, $V_{dc,b} = 22.5V$, and $V_{dc,c} = 30V$. The maximum synthesizable phase voltage in linear is

$$V_{ph_{\text{max}}} = \frac{22.5 + 15}{\sqrt{3}} = 21.65V$$  \hspace{1cm} (18)

The voltage references are given by

$$v'_{a2} = V_{ph_{\text{max}}} \sin(100\pi t)$$
$$v'_{b2} = V_{ph_{\text{max}}} \sin(100\pi t - 2\pi/3)$$
$$v'_{c2} = V_{ph_{\text{max}}} \sin(100\pi t + 2\pi/3)$$
It is applied to the modulators of the inverter in open loop. Fig. 4 compares the voltage vector spaces and the voltage trajectories in the $\alpha-\beta$-axes of traditional SPWM, traditional SVPWM, and the proposed NVM method under the given simulation condition. Compared to the balanced dc-link case, the area of the voltage vector space is reduced under the unbalanced dc-link condition. In the figure, the traditional SPWM shows the worst voltage distortion and the minimum voltage vector space. The traditional SVPWM gives more area than SPWM, but still, the voltage distortion is not avoidable. The proposed method shows no distortion on the output voltage and maximizes the voltage vector space compared to other methods. When traditional SPWM is applied, $v_{sn}^*$ is zero, and the pole voltage references are identical to the ones in eqn (18). With traditional SVPWM, $v_{sn}^*$ is no longer zero, and the peak voltage of the pole voltage references is reduced compared to SPWM. However, the duty reference of phase $a$ where the dc-link voltage is minimum among the three phases, is saturated in both cases.

Fig. 4 Comparison of the voltage vector trajectories.

Whereas with the proposed method, the fundamental frequency component of the neutral voltage is included in $v_{sn}^*$ and the duty references are not saturated. The benefit of the proposed method can also be observed from the peak value of the phase current in the fig. 11. Using traditional methods, the phase currents are unbalanced. However, the phase currents are well balanced with the proposed method. From the simulation results, it can be seen that the proposed method can synthesize the maximum available phase voltage in the linear modulation range under unbalanced dc-link conditions.

6. Simple 3-level cascaded H-bridge inverter model

Simple 3-level cascaded H-bridge inverter model is shown in Fig. 5. In this figure there are two neutral points $s$ and $n$. The voltage between the output point of each phase and the neutral point $n$ is defined as the pole voltage. The voltage between the output point of each phase and the load side neutral point $s$ is specified as the phase voltage. Here a neutral voltage between the two neutral points’ $n$ and $s$ is modulated to compensate the output voltage imbalance caused by unbalanced dc-link conditions.

Fig. 5 Simple 3-level cascaded H-bridge inverter model.

The model shown in Fig. 6 helps in generating gating signal from the duty references. Thereby the pole voltage references will be converted to PWM duty references.

Fig. 6 Model to generate gating signal from duty references.

Fig. 7 Generation of Pole voltage and Offset voltage references

Simulation model for generating pole voltages and off-set voltage references of a 3-level three phase cascaded H-bridge inverter are shown in Fig. 7. Here
the pole voltage references are generated and stated as Van, Vbn, and Vcn.

7. Results obtained for 3-level H-bridge inverter

In the exhibits of results obtained as depicted in below figures 8 to 11, traditional SPWM method is used for the variations during t=0 sec to 5 sec, traditional SVPWM method is used for the variations during t= 5 sec to 10 sec and the proposed method is used for the variations during t= 10 sec to 15 sec.

Variations of the pole voltage references obtained for the three methods are shown in Fig. 8. Here the pole voltage references in the traditional SPWM method are identical due to zero offset voltage, but in the traditional SVPWM method the pole voltages are reduced compare to SPWM because the offset voltage is no longer zero and in the proposed NVM method the pole voltages are non-uniform compared to SVPWM due to the offset voltage.

Fig. 8 Pole voltage references of 3-level H-bridge inverter.

Variations of the Offset voltage references obtained for the three methods are shown in Fig. 9. Here the Offset voltage references considered when traditional SPWM is applied are, \( v_{sn}^* \) is zero, with traditional SVPWM, \( v_{sn}^* \) is no longer zero and proposed NVM it is no longer zero.

Fig. 9 Offset voltage references of 3-level H-bridge inverter.

Variations of the duty references obtained for the three methods is shown in Fig. 10. Here the duty reference of phase a, where the dc-link voltage is minimum among the three phases, is saturated in both cases. Whereas with the proposed method, the fundamental frequency component of the neutral voltage is included in \( v_{sn}^* \), and the duty references are not saturated. The benefit of the proposed method can also be observed from the peak value of the phase current.

Fig. 10 Duty references of 3-level H-bridge inverter.

Variations of the phase currents in 3-level cascaded inverter obtained for the three methods are depicted in Fig. 11. Under traditional methods, the phase currents are unbalanced due to non consideration of neutral voltage. If the dc links in an MLCI are unbalanced and the traditional offset voltage injection methods are utilized, the three-phase output voltages may become distorted as the phase voltage reference approaches \( V_{ph\_max} \). This is because the traditional methods are not considering unbalanced dc-link conditions. Therefore, even if a phase can synthesize an output voltage reference in the linear modulation range, the other phases can be saturated or go into the over modulation region. In this situation, a neutral voltage can be produced by the saturated or over modulated phase. In order to resolve this issue and to synthesize the output voltage to \( V_{ph\_max} \) in the linear modulation range, the NVM technique is proposed. However, the phase currents are well balanced with the proposed method. From the simulation results, it can be seen that the proposed method can synthesize the maximum available phase voltage in the linear modulation range under unbalanced dc link condition.

8. Simple 5-level cascaded H-bridge inverter model

In the above model 3-level model was converted to 5-level model by cascading the h-bridge modules.
Simulation model of 5-level three phase cascaded H-bridge inverter is shown in Fig. 12. Here each H-bridge modules are cascaded to obtain 5-level.

Simulation model of H-bridge module to obtain 5-levels are shown in Fig. 13. Here two H-bridge are connected to obtain the desired level of output.

9. Results obtained for 5-level H-bridge inverter

In the exhibits of results obtained as depicted in below figures 14 to 17, traditional SPWM method is used for the variations during t=0 sec to 5 sec, traditional SVPWM method is used for the variations during t= 5 sec to 10 sec and the proposed method is used for the variations during t= 10 sec to 15 sec.

Variations of the pole voltage references obtained for the three methods are shown in Fig. 14. Here the pole voltage references in the traditional SPWM method are identical due to zero offset voltage, but in the traditional SVPWM method the pole voltages are reduced compared to SPWM because the offset voltage is no longer zero and in the proposed NVM method the pole voltages are non-uniform compared to SVPWM due to the offset voltage.

Variations of the offset voltage references obtained for the three methods are shown in Fig. 15. Here the offset voltage references considered when traditional SPWM is applied are, \(v_{sn}^*\) is zero, with traditional SVPWM, \(v_{sn}^*\) is no longer zero and for proposed NVM it is no longer zero.

Variations of the duty references obtained for the three methods are shown in Fig. 16. Here the duty reference of phase a, where the dc-link voltage is minimum among the three phases, is saturated in both cases. Whereas with the proposed method, the fundamental frequency component of the neutral voltage is included in \(v_{sn}^*\), and the duty references are not saturated. The benefit of the proposed method can also be observed from the peak value of the phase current.

Variations of the phase currents obtained for the 5-level cascaded inverter of three methods is depicted in Fig. 17. When compared to 3-level H-bridge inverters the output phase currents amplitude is more in the case of 5-level H-bridge inverter and are well balanced.

<table>
<thead>
<tr>
<th>Table 1</th>
<th>FFT analysis of current (%THD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output current</td>
<td>%THD</td>
</tr>
<tr>
<td>3-level H-bridge inverter</td>
<td>0.81</td>
</tr>
<tr>
<td>5-level H-bridge inverter</td>
<td>0.50</td>
</tr>
</tbody>
</table>

Table 1 shows the FFT analysis of currents (THD) in both 3-level and 5-level H-bridge inverters. It is observed that, %THD in output current is more in 3-level H-bridge inverter as compare to 5-level H-bridge inverter and too by increasing the number of levels, %THD is getting reduced.
10. Comparison of results with different modulation methods in 3-level inverter and 5-level inverter

The voltage values obtained in 3-level and 5-level three phase H-bridge inverter are shown in figures 18 and 19 respectively.

From these figures it is understood that the values obtained by implementing proposed NVM method is nearer to the references input values as compared to SPWM and SVPWM methods.

11. Conclusion

The NVM technique for MLCIs under unbalanced dc-link conditions has been proposed. In order to analyse the maximum synthesizable voltage of MLCIs, the voltage vector space has been analysed using the switching function. From the analysis, the maximum linear modulation range was derived. The proposed NVM technique is applied to achieve the maximum modulation index in the linear modulation range under an unbalanced dc-link condition as well as to balance the output phase voltages. Compared to the SPWM and SVPWM methods, the proposed technique improves the output voltage quality under unbalanced dc-link conditions.

As an extension to the proposed dissertation, 3-level cascaded H-bridge inverter is replaced with 5-level cascaded H-bridge inverter and simulated by applying proposed method and found that the output phase currents were balanced under unbalanced dc-link conditions. There was an improvement in the \%THD reduction and increase in the magnitude of the output phase currents comparatively.

REFERENCES


