Design of Low Power and Analysis of Various Topologies of SRAM Cell

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Abstract: SRAM cell is CMOS memory which consumes low power. It has less read and write time. There is always a increasing demand for operating different computer and multimedia applications. These applications requires more power and need critical performance level. Memory devices need to include high speed processors in addition to low power on chip memory. During access of memory power consumed results in considerable amount of total power consumption in microprocessor. Thus it is essential to reduce on chip memory power without effecting data stored in the memory cells. In this paper design of low power memory array and bit cell implementation and analysis of sram cells and comparing performance of different topologies of sram cells 6T, 7T, 8T, 9T, and 10T. The objective of this paper is to reduce average power, leakage power and leakage current with introduction of stack operation towards the pull down network. Hence designing the optimized sram topology with gpdk 180nm technology in cadence of various memory cells for 64 bit i.e. 8x8 from conventional 6T sram with the assertion of stack operation.

1. Introduction

From last 5 decades, CMOS devices are scaling down to achieve the better performance in terms of speed, power dissipation, size and reliability which can be done by making memories compact and faster or by decreasing size of memory i.e. SRAM (Static Random Access Memory). SRAM is a type of semi-conductor memory which uses bi-stable latching circuitry to store single bit. It is volatile in nature; it means that it holds the data as long as power supply is not cut off. SRAM plays an important role in modern mobile phones, microprocessors, microcontrollers, and computers etc. SRAM and DRAM (Dynamic RAM) both holds the data but in different manners. DRAM requires the data to be refreshed periodically in order to retain the data. SRAM does not need to be refreshed (therefore called static) as the transistors inside would continue to hold the data as long as the power supply is not cut off. The additional circuitry and timing are needed to refresh the DRAM periodically, which makes DRAM memory slower and less desirable than SRAM. As device size is scaled, random process variations significantly degrade the noise margin. As the sizing of the SRAM is in nanometer scale the variations in electrical parameters (e.g., threshold voltage, sheet resistance) reduces its steadily due to the fluctuations in process parameters i.e., density of impurity concentration, oxide thickness and diffusion depths. Considering all these effects, the bit yield for SRAM is strongly influenced by VDD, threshold voltage (Vth), and transistor-sizing ratios. Therefore, it is complicated to determine the optimal cell design for SRAM. The transistor mismatch can be described as two closely placed identical transistors have important differences in their electrical parameters as threshold voltage (Vth), body factor and current factor and make the design with less predictable and controllable. The stability of the SRAM cell is seriously affected by the increase in variability and decrease in supply voltage VDD [1].
Conceptually, an SRAM has the structure shown in Fig.1. It consists of a matrix of $2^m$ rows by $2^n$ columns of memory cells. Each memory cell in an SRAM contains a pair of cross coupled inverters which form a bi-stable element. These inverters are connected to a pair of bitlines through NMOS pass transistors which provide differential read and write access. An SRAM also contains some column and row circuitry to access these cells. The $m+n$ bits of address input, which identifies the cell which is to be accessed, is split into $m$ row address bits and $n$ column address bits. The row decoder activates one of the $2^m$ word lines which connect the memory cells of that row to their respective bitlines. The column decoder sets a pair of column switches which connects one of $2^n$ bitlines columns to the peripheral circuits.

1.1 Conventional 6T SRAM Cell Structure

(a) Architecture and working

The 6T SRAM cell can be designed by using two PMOS transistors and four NMOS transistors as shown in fig.2. It consists of two crossed coupled inverters and two access NMOS transistor M5 and M6. These two cross-coupled inverters, which are connected back to back, are used for storing one bit of information at a time (either 0 or 1). The two additional access transistors serve to control access to a storage cell during read and write operations. This access to the cell is enabled by the word line (WL) which controls these two access transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines, bit and bitbar [7]. They are used to transfer data for both read and write operations. The value of bit and bitbar is inverted. When bit is high then bitbar will be zero and vice-versa.

In the SRAM cell of fig.2., upper PMOS transistor in both the cross coupled inverter is termed as the load transistor and lower NMOS transistor in cross coupled inverter is termed as the driver transistor and the NMOS which connect the cell to the outside word will be termed as the pass transistor. An SRAM cell has three different states or operation: standby (where the circuit is idle), reading (when the data has been requested) and writing (when updating the contents)[8].
(b) Standby Mode

When word line is not asserted (word line=0), the access transistors M5 and M6 disconnect the cell from bit lines. The two cross coupled inverters formed by M1-M4 will continue to reinforce each other as long as they are connected to the supply. So when WL=0, access transistors M5 and M6 are off and data is held in the latch.

(c) Read Mode

Assume that 1 is stored at node a. The read cycle is initiated by pre-charging bit-lines to high voltage pulse, and then asserts word line high. Word line enables both the access transistor which will connect cell from the bit lines. The second step occurs when the values stored in a and b are transferred to the bit lines. One of the bit line will discharge through the driver transistor and the other bit lines will be pull up through the Load transistors toward VDD, a logical 1. If the content of the memory were a 0, the opposite would happen and bitbar line would be pulled toward 1 and bit line toward 0. Then these bit and bitbar will have a small difference of delta between them and then these lines reach a sense amplifier, which will sense which line has higher voltage and thus will tell whether there was 1 stored or 0. The higher the sensitivity of sense amplifier is faster is the speed of read operation of SRAM. Design of SRAM cell requires read stability (do not disturb data when reading). For read stability node ‘a’ must not flip and M4>>M5.

(d) Write Mode

Assume that the cell is originally storing a 1 and we wish to write a 0. To do this, the bit line is lowered to 0V and bit bar is raised to VDD, and cell is selected by raising the word line to VDD. Each of the inverters is designed so that PMOS and NMOS are matched, thus inverter threshold is kept at VDD/2. To write 0 at node a, M5 operates in saturation. Initially, its source voltage is 1. Drain terminal of M4 is initially at 1 which is pulled down by M5 because access transistor M5 is stronger than M1. Now M2 turns on and M3 turns off, thus new value has been written which forces bit line lowered to 0V and bit bar to VDD. SRAM to operate in write mode must have write-ability which is minimum bit line voltage required to flip the state of the cell.

1.2 Conventional 7T SRAM Cell Structure

In 7T SRAM cell structure, the cell consists of an additional transistor placed in the ground path of a 6T SRAM cell to reduce leakage while the cell is in standby mode. In the standby mode, the bottom transistor is intended to cut-off the ground path and to eliminate the leakage paths through the inverter transistor sources but this cell cannot increase the read speed.

1.3 Conventional 8T SRAM Cell Structure

The 8T SRAM cell consists of 8 transistors, N1-N5 and P1- P3, as shown Fig. 3.Four transistors N1, N2, P1, P2 form a cross-couple structure to store data. Four transistors P3 and N3- N5 are access to the internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes to the BLs while P3 and N5 form an inverter to control the voltage of node C1. The source terminal of P3 is connected to a column select (CS) line while gates of P3 and N5 are connected to WL. Unlike conventional design, the sources of P1 and P2 are connected to dynamic cell supply (cell_supply) line which is raised to the higher voltage during read operation to obtain a higher noise margin [10]. During Read operation in 6T SRAM cell, the fundamental stability problem occurs. In order to reduce leakage power consumption, pre-charge voltage for bit-lines is kept much lower than the cell supply voltage [13]. When the transistors are turned on, the ‘0’ logic node is pulled up to a poor ‘0’ level and the ‘1’ logic node is pulled down to a poor ‘1’ level; this may lead to flip the cell data. In the 8T SRAM cell, three MOSFETs are introduced to separate the read and write current paths and to avoid the accidental flipping of cell during read operation.

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Fig 4: Cell structure of 8T SRAM Cell

2. Experimental Work
Waveform is generated by using W-Edit. The transient response of various cells is given below.

Fig 5: Transient Response of 64 bit 6T SRAM Cell.

2.1 Simulation Results of 7T SRAM Cell
The transient response of designed 7T SRAM cell is presented in fig.

Fig 6: Transient Response of 7T SRAM Cell
2.2 Simulation Results of 8T SRAM Cell

The transient response of designed 8T SRAM Cell is presented in fig. 7.

![Fig.7: Transient Response of 8T SRAM Cell](image)

2.3 Simulation Results of 10T SRAM Cell

The transient response of designed 10T SRAM cell is presented in fig. 8.

![Fig.8: Transient Response of 10T SRAM Cell](image)

2.4 Comparative Analysis Using Various Parameters

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<th>SL No</th>
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<th>7T SRAM Cell</th>
<th>8T SRAM Cell</th>
<th>9T SRAM Cell</th>
<th>10T SRAM Cell</th>
<th>Modified 64 bit 6T SRAM</th>
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Table 1 Performance parameter of various SRAM Cell Structure.
2.5 Conclusion
It has been concluded that if the number of transistor is increased in the SRAM cell the power dissipation will be increased due to increase in area, but other parameter like noise, delay can be reduced during read and write operation. So the optimum case is taken between speed, power and area.

4. References


