SQNR and Sampling Frequency Analysis of 4\textsuperscript{th} order VCO- Based ADC using Phase Detector as a Loop Filter

Abhishek Kumar Prajapati\textsuperscript{1}, Ayoush Johari\textsuperscript{2}, Rakesh Agarwal\textsuperscript{3}
\textsuperscript{1,2,3}Dept. of Electronics & Communication Engineering
Lakshmi Narain college of Technology and Science, Bhopal, India

Abstract: This paper presents the SQNR and sampling frequency analysis of 4\textsuperscript{th} order VCO based ADC. The 4\textsuperscript{th} order VCO-ADC has been explored on 50 nm MOCMOS technology which measures SQNR of 76.8 dB over 127 GHz frequency and 304.8 GHz sampling frequency using 5V supply. The quantization error has been fed in the feedback loop to perform the noise shaping.

1. Introduction

In a signal transmission there is often need to convert data at both the ends i.e. analog signal to digital and vice-versa. In this category the analog to digital converters are called as ADC and the digital to analog converters are called as DAC. VCO is one of the most important basic building blocks in analog and digital circuit. Among the different types of ADC i.e. Sigma-delta ADC, Successive approximation ADC, Flash ADC, Direct conversion ADC the VCO based ADC is one of the most promising analog to digital converter (ADC). The delta-sigma ADC which is ring VCO based has many advantages for which it is preferred when compared with the conventional ADCs i.e. in the order of magnitude, reduction in the chip area, reduced complexity in the circuit design which is achieved by replacing many of the analog and digital blocks by only a ring VCO. With these advantages there are some inevitable disadvantages in which the primary one is the severe nonlinearity of the $K_v$ (the voltage to frequency conversion coefficient of the VCO), which limits the linearity of the circuit as well as the output signal.

The characteristic of a VCO as a CT voltage-to-phase integrator makes it relevant in the design of Continuous time sigma-delta ADC’s i.e. CT $\Sigma\Delta$ ADC’s. Like CMOS digital gate, the VCO output itself toggles between two discrete levels, $VDD$ and GND, the VCO output phase and frequency are continuously varying.

VCO based ADC suffers with severe non-linearities which limits the noise shaping property of the signal which results in the less SNR, SQNR value of the circuit. The value of the SNR, SQNR increases with the increase in the order of the VCO-ADC circuit. With the increased VCO-ADC order certain non-linearities gets eliminated.

2. Background

As its clear from [1],[2],[3], the nonlinearity poses a severe challenge towards achieving high SNR and SQNR value in VCO ADC structure. The phase is used as the key output variable rather then the frequency of the quantizer, in the 4\textsuperscript{th} order VCO-ADC. In practice, thermal noise, DAC mismatch, and other noise and error terms will add on top of the quantization noise floor and further degrade SNDR.

In order to achieve the performance target of SNDR 70dB, it is necessary to achieve higher order quantization noise shaping by extending the loop filter beyond first-order. The nonlinearity in the VCO’s voltage-to-frequency ($K_v$) transfer characteristic seriously limits the resolution of VCO-based ADCs as shown in Fig. 1.

The resolution of the VCO based ADC is limited by the nonlinearity in the VCO’s voltage-to-frequency ($K_v$) transfer characteristic which has been shown in Fig. 1. While the circuit in Fig. 2 improves before the VCO and employing negative feedback, nonlinearity still limits resolution to less than 11 ENOB in a 20MHz bandwidth. The resolution of prior VCO based ADC’s was primarily limited by the distortion arising from the VCO $K_v$ non-linearity. While negative feedback techniques helped to suppress the distortion by more than an order of magnitude, non-linearity still prevented the ADC from achieving its full dynamic range.
The work in [6],[8],[9] shows how the linearity of the circuit was limited mostly between 30-50 dB by severe non-linearities of the published designs. A continuous time delta sigma (CT-ΔΣ) architecture proposed in [11] achieved second order noise shaping by preceding the multi-phase VCO quantizer with an op-amp based integrator, and using a multibit feedback DAC. The Discrete time(DT) ΔΣ architecture in [12] tried to bypass a multibit DAC implementation and the required dynamic element matching (DEM) overhead by using a frequency difference detector that pulse-width modulated a one-bit DAC. However, this approach had additional complexities in the frequency difference detector design, and lost the inherent first-order noise-shaping provided by the VCO quantizer. A modified version of the ADC in [13] was actually implemented and provided measured results in [14]. Ref [14] shows that the third-order CT ΔΣ ADC achieved an extra order of noise shaping without a second op-amp integrator by creating a passive pole with a large on-chip capacitor. Fig 1 shows the third order noise shaping of VCO-ADC. As any feedback loop functions as a filter, the noise shaping works by putting the quantization error in a feedback loop, so by creating feedback loop for error itself, the error can be filtered as desired.
3. 4<sup>th</sup> Order VCO-ADC

The 4<sup>th</sup> order VCO based ADC [12] exhibits the SNR value of greater than 70 dB which exhibits that the circuit is less affected by the non-linearities present in the circuit. This circuit doesn't show any value of SQNR. In [12] the circuit is implemented using VCO quantizer, RZ DAC, NRZ DAC, and the loop filter. As it's quite clear till now that the noise shaping of the circuit can be improved by comprising a closed loop system and in this circuit when the quantization noise is fed back to a closed loop system the noise shaping property of the circuit is improved. To obtain the desired frequency response the loop filter is made tunable. The feedback path is implemented as a feedback DAC by using either NRZ or RZ DAC. RZ DAC is used within the minor loop feedback since any quantization noise folding arising from VCO $K_v$ non-linearity will be suppressed by the open loop gain of the loop filter. The result showed the SNR value and SNDR value as 81.2 dB and 78.1 dB respectively over 20 MHz bandwidth.

Effective number of bits i.e. ENOB is the measure of the ADC and its associated circuitry and can be described as the resolution of ADC. This paper presents the work which deals with the ENOB=12. By extending the loop filter we can achieve higher order quantization noise shaping which will give the value of SQNR > 70 dB which will make it clear that the circuit can be made free from non-linearities even with the less number of ENOB.

4. Circuit Design And Simulations

The circuit mainly consists of four blocks among which the PD works as a loop filter. The output of the PD is been combined with the RZ DAC and NRZ DACs output and is fed to the quantizer as an input through the adder. The presented work uses PD i.e. phase detector as a loop filter with the simplified RZ DAC and NRZ DAC configurations. PD generates an output signal whose phase is related to the phase of an input signal. Keeping the input and output phase in lock step also implies keeping the input and output frequency the same.

4.1 Phase Detector

The two input signals is been compared by the PD which an error signal which is proportional to their phase difference. The error signal is low pass filtered and used to drive a VCO which creates output phase. The basic schematic of the phase detector is shown in the Fig. 5.
4.2 RZ DAC

Here the RZ DAC is used as a minor feedback loop due to its heightened sensitivity to clock jitter. RZ DAC is a delay compensating DAC in order to absorb the propagation delay of the quantizer as shown in Fig. 6. The bandwidth of RZ DAC is almost twice when compared with its NRZ counterpart, requiring high power DAC switch buffers. Errors in the minor-loop DAC are suppressed by the gain of the PD.

4.3 NRZ DAC

To make the converter less sensitive to clock jitter the multibit NRZ DAC structure which is shown in Fig. 7. is adopted as a main feedback loop. Due to the phase detector gain, the mismatches in minor loop DAC are not as serious as those in main NRZ feedback DAC.

4.4 VCO Quantizer

The VCO delay element in VCO quantizer is based on the current starved inverter from [16], and enables full swing output signals of the output frequency. Current steering RZ and NRZ DAC are implemented for their fast switching speeds. The SNR degradation due to clock jitter can be reduced significantly by pursuing a multibit quantizer and NRZ feedback DAC implementation [13-16].

5. Methodology Used

The systematic design methodologies are necessary for converters circuits to perform correctly. The design of VCO-ADC consists of different blocks i.e. phase detector, VCO, ADC, DAC and adders.

Standard topologies are used in the initial designing of the circuit, then the parasitic is decided, parameters are decided, the process technology is chosen and circuits are simulated if not found ok are changed and re-simulated for numerous topologies selected.

6. Result

![Figure 10. FFT presentation of 4th order VCO-ADC using phase detector as a loop filter](image)
## Parameters

<table>
<thead>
<tr>
<th>VCO ADC type</th>
<th>Present Work</th>
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<tbody>
<tr>
<td>2\textsuperscript{nd} order ADSM</td>
<td>50 nm MOCMOS</td>
</tr>
<tr>
<td>2\textsuperscript{nd} order ADC (ADSM + VCO)</td>
<td>2\textsuperscript{nd} order VCO-ADC with feedback loop</td>
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<tr>
<td>4\textsuperscript{th} order VCO-ADC</td>
<td>4\textsuperscript{th} order VCO-ADC</td>
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The simulation and the FFT analysis of the above presented prototype has been performed on the LTspice simulator and the result is shown in Fig. 10. above. The tabular representation comparing different parameters of all the priors work has been compared in the Table 1 above. This work mainly focuses on the sampling frequency and SQNR calculation. By creating the above prototype of 12-bit we have succeeded in achieving SQNR>70 dB and the output more free from noise even at the low ENOB compared with the previous 4\textsuperscript{th} order VCO-ADC circuit [2], as this was the main objective of our work.

## 7. Acknowledgment

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## 8. Conclusion

In this paper we have presented the 12-bit 4\textsuperscript{th} order VCO based ADC using phase detector as a loop filter using 50nm MOCMOS technology. With the presented prototype we have achieved SQNR value of 76.8 dB over 127 GHz bandwidth. The sampling frequency achieved from the 127 GHz bandwidth is 304.8 GHz. Here we are dealing with the GHz frequency range. The SQNR with such a value supposed to have output free from noise. With this circuit we have also achieved the output free from non-linearities as compared with all the previous VCO-ADC designs.

## References


[10] Matthew Park and Michael H. Perrott. “ A 78 dB SNDR 87 mW 20 MHz Bandwidth Continuous-Time _0.5 ADC With VCO-Based Integrator and Quantizer Implemented in 0.13 micron CMOS” IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 12, DECEMBER 2009


