High Performance MAC Design Based on Vedic Multiplication and Reversible Logic Gates

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Abstract—Variable latency adders have been as of late proposed in writing. A variable latency adder utilizes speculation: the correct math function is supplanted with an approximated one that is speedier and gives the right outcome more often than not, however not generally. The approximated adder is enlarged with a mistake discovery network that asserts a blunder flag when speculation falls flat. Speculative variable latency adders have pulled in solid interest thanks on account of their ability to lessen normal postpone contrasted with conventional structures. This paper proposes a novel variable speculative theoretical prefix topology that came about more successful than variable inactivity Kogge-Stone topology. The paper describes the phases in which variable idleness theoretical prefix adders can be subdivided and displays a novel mistake recognition organize that lessens blunder likelihood contrasted with past methodologies. A few variable idleness theoretical adders, for different operand lengths, utilizing both Han-Carlson and Kogge-Stone topology, have been blended utilizing the UMC 65 nm library. Acquired outcomes demonstrate that proposed variable inactivity Han-Carlson viper outflanks both already proposed theoretical Kogge-Stone designs and non-speculative adders, when rapid is required. It is likewise demonstrated that non-speculative adders remain the best decision when the speed constraint is casual.

Index Terms—Addition, digital arithmetic, parallel-prefix adders, speculative adders, speculative functional units, variable latency adders.

I. INTRODUCTION

Vedic Mathematics is a standout amongst the oldest philosophies utilized by the Aryans with a specific end goal to perform numerical calculations. This comprises of algorithms that can boil down huge number arithmetic operations to straightforward personality calculations. The above said advantage originates from the way that Vedic arithmetic approach is entirely unexpected and considered near the way a human personality works. The endeavors put by Jagadguru Swami Sri Bharati Krishna.Tirtha Maharaja to acquaint Vedic Mathematics with the normal people and streamline Vedic Algorithms into 16 classifications or Sutras should be recognized and acknowledged. The Urdhv a Tiryakbhayam is one such augmentation calculation which is outstanding for its productivity in diminishing the calculations included.

A. Background

Adders are fundamental elements in arithmetic operations. Binary adders are utilized as a part of digital circuit for addition, subtraction operations and for floating point multiplication and division. Therefore adders are Fundamental components and improving their performance is one of the major challenges in digital designs. Computer arithmetic algorithm has established lower bounds on area and delay of n-bit adders, the former varies linearly with adder size, and the latter has an O (log2 (n)) behavior. High speed adders depend on entrenched parallel prefix structures including Brent-Kung [1], Kogge-Stone [2], Han-Carlson [3]and soon. These standard structures work with fixed latency. Better average performances can be achieved by using variable latency adders that have been recently proposed in literature speeding up of approximate circuits. The approximated adder is enlarged with error detection network that asserts error signal when hypothesis fails. In this case (Mis prediction), another clock cycle is needed to obtain the correct result with the help of a correction stage. Since the addition time is one clock cycle when no error happens and two clock cycles when the speculation fails. A first theoretical way to deal with expansion was proposed by Nowick [4] in asynchronous challenge, which executes a variable latency adder cutting the least levels of a Kogge-Stone adder. In synchronous challenge, Verma [5] propose a variable latency speculative adder cutting the lower levels of a Kogge-Stone adder. The Kogge-Stone adder is frequently utilized when velocity is the essential worry has fan-out of This comes at the expense of utilizing numerous propagate-generate cells and numerous wires that must be directed between stages.

With the advancement in the VLSI innovation, there is a ever expanding extinguish for convenient and
2. LITERATURE SURVEY

Energy disperses at whatever point exchanging movement happens in the CMOS circuits. Landauer’s Principle expresses that consistent calculations that are not reversible necessarily create k*T*ln(2) joules of warmth vitality, where k is the Boltzmann’s Constant k=1.38x10^-23 J/K, T is the total temperature at which the calculation is performed. In spite of the fact that this measure of warmth seems, by all accounts, to be little, Moore’s Law predicts exponential development of warmth produced because of data lost, which will be a discernible amount of warm loss in one decade from now. [1]

Bennett demonstrated that zero vitality dissemination would be possible just if the system comprises of reversible rationale doors. Thus reversibility will turn into a basic prop-erty in future circuit outline innovations. Reversible circuits are those circuits that don't free data. Reversible calculation in a framework can be performed just when the framework involves reversible gates. [2]

A first speculative approach to addition was proposed by Nowick [12] in asynchronous contest, which implements a variable latency adder cutting the lowest levels of a Kogge-Stone adder. In synchronous contest, Verma et al.[13] propose a variable latency speculative adder; here the speculative addition is realized in the same way as [12], cutting the lower levels of a Kogge-Stone adder. A similar approach is employed in [4].

In [15] a variable inertness carryselect snake is presented, where the viper is divided in different windows, every one containing a Kogge-Stone viper. The Kogge-Stone viper is frequently utilized when speed is the essential worry, since it utilizes the base number of rationale levels and every cell in the snake tree has fanout of 2. This comes at the cost of utilizing many spread produce cells and many wires that must be steered between stages. [5]

In this paper we propose a novel variable latency speculative adder in view of Han-Carlson [6] parallel-prefix topology. The Han-Carlson topology utilizes one more stage than Kogge-Stone viper, while requiring a decreased number of cells and streamlined wiring. In this manner, it can accomplish comparative speed execution contrasted with Kogge-Stone snake, at lower control utilization and zone [16]. We demonstrate that a theoretical convey tree can be acquired by pruning some middle of the road levels of the traditional Han-Carlson topology. The paper introduces a thorough determination of the mistake discovery system and demonstrates that the blunder location arrange required in theoretical Han-Carlson adders is fundamentally quicker than the one utilized by speculative Kogge-Stone design. [6]

The paper is organized as follows. In Section II we review the essential engineering of parallel-prefix adders. The phases in which variable inertness theoretical prefix adders can be subdivided are displayed in Section III where, after a concise audit of Kogge-Stone theoretical prefix-handling stage presented in [12], we exhibit the proposed Han-Carlson speculative topology. Point by point exchange about the blunder discovery stage is additionally detailed in this Section. The Section IV presents spatial and timing complexity of investigated architectures. It shows detailed implementation and synthesis results of the proposed adders, for operand size ranging from 32 through 128 bits. Section VI concludes the paper with some final remarks. In paper published by M.Sindhura and Niranjan they design MAC unit using Wallace multiplier and look ahead carry but the
performance of adder is still not satisfactory as look ahead carry requires high power and area. [7]

In paper H. Thapliyal and M.B. Srinivas composed the multiplier utilizing two units; one is the halfway item era unit built utilizing Fredkin doors and other the summing unit developed utilizing 4x4 TSG entryways has proposed a plan of reversible multiplier which makes utilization of Peres door for era of incomplete items when contrasted with which utilizes Fredkin doors. For the development of adders the HNG entryway was conceived. Proposes low quantum cost realization of reversible multipliers which principally utilizes Peres full snake entryway (PFAG) for its outline. In paper distributed by Rakshit Saligram they Design MAC utilizing vedic Multiplier and reversible entryways however riiple convey .But because of swell convey the execution of snake gets poorer as no bits to be include increments . So We propose another plan with vedic multiplier and variable idleness theoretical Han-Carlson snake which gives Better execution than above techniques. [8]

3. METHODOLOGY

3.1 Multiplication Methods

3.1.1 URDHVA TIRYAKBHAYAM MULTIPLICATION ALGORITHM

Urdhva Tiryakbhayam (UT) is a multiplier in view of Vedic mathematical algorithms devised by antiquated Indian Vedic mathematicians. Urdhva Tiryakbhayam sutra can be connected to all instances of duplications viz. Parallel, Hex and furthermore Decimals. It depends on the idea that era of every single fractional item should be possible and after that simultaneous expansion of these incomplete items is performed. The parallelism in era of fractional items and their summation is acquired utilizing Urdhva Tiryakbhayam. Dissimilar to different multipliers with the expansion in the quantity of bits of multiplicand as well as multiplier the time delay in calculation of the item does not increment proportionately. On account of this reality the season of calculation is free of clock recurrence of the processor. Consequently one can confine the clock recurrence to a lower esteem. Likewise, since processors utilizing lower clock recurrence scatter bring down vitality, it is efficient as far as power variable to utilize low recurrence processors utilizing quick algorithms like the previously mentioned. The Multiplier in view of this sutra has the preferred standpoint that as the quantity of bits increases, gate delay and area increases at a slow pace.

3.1.2 OPTIMIZATION OF THE URDHVA TIRYAKBHAYAM MULTIPLIER

The conventional logic plan execution of a 2x2 Urdhva Tiryakbhayam multiplier utilizing the irreversible rationale entryways [8] is an appeared in the Figure 3. In [12] the four expressions for the yield bits are gotten from this figure and is utilized to get the reversible execution as appeared in Figure 4. The circuit utilizes five Peres doors and one Feynman entryway. This plan has an aggregate quantum cost of 21, number of refuse yields as 11 and number of steady sources of inputs 4. The entryway tally is 6. This outline does not mull over the fan outs. The general execution of the UT multiplier is scaled up by improving every individual unit as far as quantum cost, garbage outputs and so on.

![Fig. 01 Vedic Multiplication](image)

![Fig. 02 Hardware Realization of 2 * 2 Block](image)

3.2 Reversible Gates

A Reversible Logic gate is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. This not only helps to determine the outputs from the inputs but also the inputs can be particularly recovered from the yields. As a result of this bijective mapping the output vectors are simply stages of the input vectors. Some of the essential reversible
rationale doors in the literature those are valuable in designing the Reversible Urdhva Tiryakbhayam Multiplier are the Feynman [5] Gate—the main 2x2 entryway, that is utilized for fan-out purposes and additionally to complement. It has a quantum cost of one. Peres [6] Gate—a 3x3 door that is utilized to deliver AND operation and also EX-OR operation. It has a quantum cost of four. New Fault Tolerant door (NFT) — is likewise a 3x3 entryway with a quantum cost five. HNG door which is a 4x4 entryway that can be adequately utilized as a full snake and gives least quantum cost usage. It has a quantum cost of six. BVPPG [11] is a 5x5 door with a quantum cost of ten.

Fig 03 Optimization parameters for reversible logic circuits

The important parameters [14] which assume a noteworthy part in the outline of a optimized reversible rationale circuit are as recorded:

1. Constants (CI): This refers to the quantity of number of inputs that are to be kept up consistent at either 0 or 1 in request to combine the given logical function.

2. Garbage (GO): This refers to the quantity of pads which are not utilized as a part of the combination of a given function. These are extremely basic, without which reversibility can't be accomplished.

3. Gate tally (NG): The quantity of reversible gates used to understand the capacity.

4. Flexibility: This refers to the all-inclusiveness of a reversible rationale door in acknowledging more functions.

5. Quantum cost (QC): This alludes to the cost of the circuit as far as the cost of a primitive door. It is ascertained knowing the quantity of primitive reversible rationale entryways (1x1 or 2x2) required to understand the circuit.

6. Gate levels: This refers to the quantity of levels in the circuit which are required to understand the given rationale capacities.

7. Total Reversible Logic Implementation Cost (TRLIC) [12]: Let, in a reversible rationale circuit there are NG reversible rationale entryways, CI consistent sources of info, GO number of refuse yields, and have a quantum cost QC.

**2x2 REVERSIBLE VEDIC MULTIPLICATION BY USING URDHVA TIRYAKHYAM(UT):**

![Diagram of 2x2 Multiplier](image)

**Fig. 04. 4x4 Multiplier using 2x2 multiplier**

**3.2 Adder**

ADDERS are essential functional units in PC arithmetic. Binary adders are utilized as a part of woprocess or for expansion and subtraction operations and also to float point multiplication and division. In this manner adders are basic parts and enhancing their execution is one of the real difficulties in advanced outlines. Hypothetical research [1] has set up lower limits on location and deferral of - bit adders: the previous differs straightly with viper measure, the last has a conduct.

High speed depend on entrenched parallel prefix designs [1], [2], including Brent-Kung [3], Kogge-Stone [4], Sklan sky [5], Han-Carlson [6], Ladner-Fischer [7], Knowles [8]. These standard designs work with settled dormancy. Better normal exhibitions can be accomplished by utilizing variable inactivity adders that have been as of late proposed in writing [9]. A variable idleness viper utilizes hypothesis: the correct number-crunching capacity is supplanted with an approximated one that is speedier and gives the right outcome more often than not, yet not generally. The approximated viper is increased with a mistake recognition arrange that affirms a yield signal when hypothesis fizzes. For this situation (misprediction), another clock cycle is expected to get the right outcome with the help of a correction stage.

The pre-processing and post-processing phases of a prefix viper include just straightforward operations on signs nearby to each piece position. Accordingly,
viper execution basically relies upon prefix-processing stage. It indicates Han-Carlson and Kogge-Stone prefix adders’ topologies.

![Han-Carlson adder and Kogge Stone Adder parallel prefix topologies](image1)

Here dark dots speak to the prefix administrator, while white spots are basic placeholders. Kogge-Stone viper is created by levels and present a fanout of two at each level utilizing an expansive number of dark cells and many wire tracks. A decent exchange off between fanout, number of rationale levels and number of dark cells is given by Han-Carlson. The external lines of the Han-Carlson topology are Brent-Kung [3] charts, while the inward columns are Kogge-Stone diagrams. The Han-Carlson viper in Fig. 1 utilizes a solitary Brent-Kung level toward the start and toward the finish of the graph, and the number of levels is 1+log2n.

**Proposed Design Process of the MAC in view of FPGA is:**

1. To review the multiplier with their advantages and confinements.
2. To review the adder with their advantages and confinements.
3. Making examination compose verilog code. Implementation and Synthesis on the Xilinx
4. ISE Design Suit 14.7, ISim simulator
5. After synthesisation watch the simulation comes about.

**Software to be use:**

1. Xilinx ISE Design Suit 14.7, ISim simulator
2. FPGA Development board: Xilinx Artix-7KIT
3. Altera Quartus II ModelSim 10.1d

**4. EXPERIMENTAL RESULT**
CONCLUSION

In this paper a novel variable latency Han-Carlson parallel prefix speculative adder for high-speed application is proposed. A new, more accurate, error detection network is introduced, which allows reducing the error probability compared to the previous approaches. An extensive set of implementation results for 65 nm CMOS technology shows that proposed Han-Carlson variable latency adders outperforms previously developed variable latency Kogge-Stone architectures. Compared with traditional, non-speculative, adders, our investigation exhibits that variable inertness Han-Carlson adders indicate sensible enhancements when the most elevated speed is required; generally the weight forced by mistake recognition and blunder rectification stages overpowers any favorable position. Extra work is required to extend the theoretical way to deal with other parallel-prefix models, for example, Brent-Kung, Ladner-Fisher, and Knowles.

REFERENCES