Design and Characteristic Analysis of Gate All Around Nanowire MOSFET and Its Application

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Abstract: The Gate-All-Around nanowire MOSFET structure is a device that is designed to give high performances. It has a good future scope as could be used in the ultra scale integration. When the scaling is done at a very few nanometer planar structure are not effective, as this device has a surrounding gate it give a better electrostatic control. It give high \(I_{on}\) to \(I_{off}\) ratio, reduces delay and short channel effect. This paper describes a Gate-All-Around nanowire MOSFET at 20nm for both Nmos and Pmos and its characteristics. It is also compared with the conventional MOSFET. The substrate material used is silicon. The substrate material is changed with iii-v group materials like AlGaAs and its effects are shown. The effect of scaling in doping (overlap and underlap doping), effect of variation in oxide thickness are shown. This device is then being used to make applications CMOS inverter, NAND gate, NOR gate, OR gate, AND gate and 3 stage ring oscillator.

Keyword: GAA NW MOS (Gate-All-Around nanowire MOSFET), SCE (short channel effect)

[I] INTRODUCTION

Silicon nanowire MOSFET uses narrow silicon channel for the enhancement of electrostatic controllability of its channel. Therefore, they have lower \(I_{off}\) and higher \(I_{on}\) values. High On-current is important for reduction of delay time because circuit operation is determined by the charging time of the next stage capacitance. Therefore high on-current is required for high speed operation of the circuit. The Gate all around (GAA) structure achieves the criterion using the smallest gate length at the same silicon thickness. On the other hand, the largest silicon body thickness is allowed to achieve the criterion at the same gate length. Therefore the immunity of the GAA structure for the short channel effect is the largest. As the silicon body thickness decreases the smaller gate length can be used. Therefore the SiNW MOSFET, which has small diameter of silicon channel, has the largest advantage. Also Silicon nanowire MOSFET has high effective carrier mobility.

The short channel effect appears as the gate length of MOSFET decreases. The Gate-All-Around nanowire MOSFET has gate all around surface so they have less SCE.

[II] DEVICE STRUCTURE

The Gate-All-Around nanowire MOSFET structure is as shown in figure below. Parameters of the device are:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Length</td>
<td>20nm</td>
</tr>
<tr>
<td>Length of Source and Drain</td>
<td>10nm</td>
</tr>
<tr>
<td>Source and Drain Thickness</td>
<td>1nm</td>
</tr>
<tr>
<td>Gate Material</td>
<td>NpolySi</td>
</tr>
<tr>
<td>Donor Concentration</td>
<td>(1 \times 10^{20} , \text{cm}^{-3})</td>
</tr>
<tr>
<td>Acceptor Concentration</td>
<td>(5 \times 10^{18} , \text{cm}^{-3})</td>
</tr>
<tr>
<td>Oxide Thickness</td>
<td>2nm</td>
</tr>
</tbody>
</table>
[III] RESULTS

To verify the proposed analytical model, the simulator VISUAL TCAD version 1.9.0-a1 has been used to simulate the different aspects such as effect of scaling in doping, changing oxide thickness, using iii-iv group elements as substrate material instead of silicon.

1. **I_D versus V_GS** :-

The transfer characteristic of MOSFET relates drain current response to the input gate source voltage. Since the gate terminal is electrically isolated from the remaining terminals, the gate current is essentially zero, so the gate current is not a part of device characteristic.
Figure 3 For PMOS type GAA NW MOS ($I_D$ versus $V_{GS}$)

$2 \ I_D \ versus \ V_{DS}$:

Figure 3 For NMOS type GAA NW MOS ($I_D$ versus $V_{DS}$)
The Gate-All-Around nanowire MOSFET is a three dimensional device hence it does not follow the current equations of the planer MOS devices. The current equation for this device is derived Landauer-Buttiker formula and according to it the current equations for device are as follows.

**FOR CUT OFF REGION**

\[ I_d = 0 ; \quad V_{gs} < V_t \]

**FOR TRIODE REGION**

\[ I_d = \frac{e^2}{\pi \hbar} 2 \frac{W R}{l_{ch}} \left( v_{gs} - v_t \right) v_{ds} - \frac{1}{2} v_{ds}^2 \]

\[ V_{ds} < V_{gs} - V_t \]

**FOR SATURATION REGION**

\[ I_d = \frac{e^2}{\pi \hbar} \frac{W R}{l_{ch}} \left( v_{gs} - v_t \right)^2 \]

\[ V_{ds} \geq V_{gs} - V_t \]

Where \( \frac{e^2}{\pi \hbar} \) is a laplace limit of current.
The fig-5 shows that the GAA NW MOS has better ON current to OFF current ratio. The values are given in the following table.

**TABLE- 1 ON current and OFF current and its ratio**

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>$I_{ON}$</th>
<th>$I_{OFF}$</th>
<th>$I_{ON}/I_{OFF}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>GAA- NW- MOS</td>
<td>0.00106459</td>
<td>$1.1963\times10^{-11}$</td>
<td>$8.89\times10^7$</td>
</tr>
<tr>
<td>NMOS</td>
<td>0.000438799</td>
<td>$3.8880\times10^{-10}$</td>
<td>$1.128\times10^6$</td>
</tr>
</tbody>
</table>

### [VI] DEVICE VARIATIONS

#### [a] EFFECT OF DOPING

Here the doping is scaled length wise. The doping can be either under lap scaled or overlap scaled doping. In this device we scaled the doping by 2nm i.e. by 1nm each side of acceptor region. If towards the donor region then it is overlap scaled if away from the donor region then it is called under lap scaled.

#### (i) OUTPUT OF SCALING IN DOPING
Figure 6 shows the graph between drain current and gate to source voltage at constant drain to source voltage which is taken here 0.1 volt. The $V_{gs}$ is swept from 0 to 1 volt and a step voltage of 0.05 volt is applied. The graph is produced at different conditions. The conditions are under lap, overlap and no change. It can be seen from the table 2 that the on current to off current to ratio is better for overlapped scaling. The result shown here are for nmos type GAA NW MOS.

(ii) EFFECT IN $I_{ON}$ TO $I_{OFF}$ RATIO

<table>
<thead>
<tr>
<th>CONDITION</th>
<th>$I_{on}$</th>
<th>$I_{off}$</th>
<th>$I_{on}/I_{off}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Under lap</td>
<td>0.000336985</td>
<td>3.19412e-09</td>
<td>105501.6718</td>
</tr>
<tr>
<td>No change</td>
<td>0.000335822</td>
<td>3.044e-09</td>
<td>110322.6018</td>
</tr>
<tr>
<td>Overlap</td>
<td>0.000287618</td>
<td>2.67381e-10</td>
<td>1075686.006</td>
</tr>
</tbody>
</table>

[b] USING III-IV GROUP ELEMENT INSTEAD OF SILICON

The iii-iv group elements have higher carrier mobility hence they have better on current to off current ratio.

316671.672, 110318.977
FIGURE 7 COMPARE AlGaAs WITH Si

Figure 7 shows the linear log10 scale graph between drain current and gate to source voltage at constant drain to source voltage which is taken here 0.1 volt. The \( V_{gs} \) is swept from 0 to 1 volt and a step voltage of 0.05 volt is applied. The graph is produced at different material. Clear result can be seen from the table 3 that the AlGaAs has better on to off current ratio.

<table>
<thead>
<tr>
<th>MATERIAL</th>
<th>( I_{on} )</th>
<th>( I_{off} )</th>
<th>( I_{on}/I_{off} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlGaAs</td>
<td>0.000198709</td>
<td>6.27493e-10</td>
<td>316671.672</td>
</tr>
<tr>
<td>Si</td>
<td>0.000335822</td>
<td>3.044e-09</td>
<td>110322.6018</td>
</tr>
</tbody>
</table>

[c] SCALING EFFECTIVE OXIDE THICKNESS

Here we will see effects of changing the effective oxide thickness. By reducing its thickness by 1nm we observe the result.

(i) Effect on Output
FIGURE 8 EFFECT OF CHANGE IN OXIDE THICKNESS

The figure 8 clearly shows that the 1nm thickness give better result. The on current to off current value improves can be seen from the table 4.

TABLE 4 EFFECT OF CHANGING THE OXIDE THICKNESS

<table>
<thead>
<tr>
<th>MATERIAL</th>
<th>$I_{on}$</th>
<th>$I_{off}$</th>
<th>$I_{on}/I_{off}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1nm</td>
<td>0.0007311</td>
<td>2.578e-09</td>
<td>283591.9317</td>
</tr>
<tr>
<td>2nm</td>
<td>0.000335822</td>
<td>3.044e-09</td>
<td>110322.6018</td>
</tr>
</tbody>
</table>

The table shows the on and off current value at 1nm and 2nm. Reducing improves the result hence give better performance

[VII] APPLICATIONS

[A] CMOS INVERTER

(i) DEVICE STRUCTURE
FIGURE-9 CMOS INVERTER

(ii) OUTPUT OF CMOS INVERTER

(a) DC ANALYSIS

FIGURE- 10 DC ANALYSES

(b) AC or Transient analysis of CMOS inverter.
[B] NAND, NOR GATE
The device structure for NAND and NOR gate is same only interconnections are different which are internally connected

(i) DEVICE STRUCTURE

(ii) OUTPUT OF NAND GATE
(iii) OUTPUT OF NOR GATE

[C] OR, AND GATE and 3 stage ring oscillator

(i) DEVICE STRUCTURE
(ii) OUTPUT OF OR GATE

![Figure 16: Output of OR Gate](image1)

(iii) OUTPUT OF THREE STAGE RING OSCILLATOR

![Figure 17: Output of 3 S.R.O](image2)

(iv) OUTPUT OF AND GATE

![Figure: Output of AND Gate](image3)
CONCLUSION

The design and the characteristics analysis of Gate-All-Around nanowire MOSFET is successfully implemented and simulated through software “visual TCAD”. Firstly a brief introduction of the device is given. The device is designed and implemented and its results are shown. The variations are done in the device which shows improvement. The applications are implemented which use Gate-All-Around nanowire MOSFET as the base device and the output of each applications are shown.

REFERENCES


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